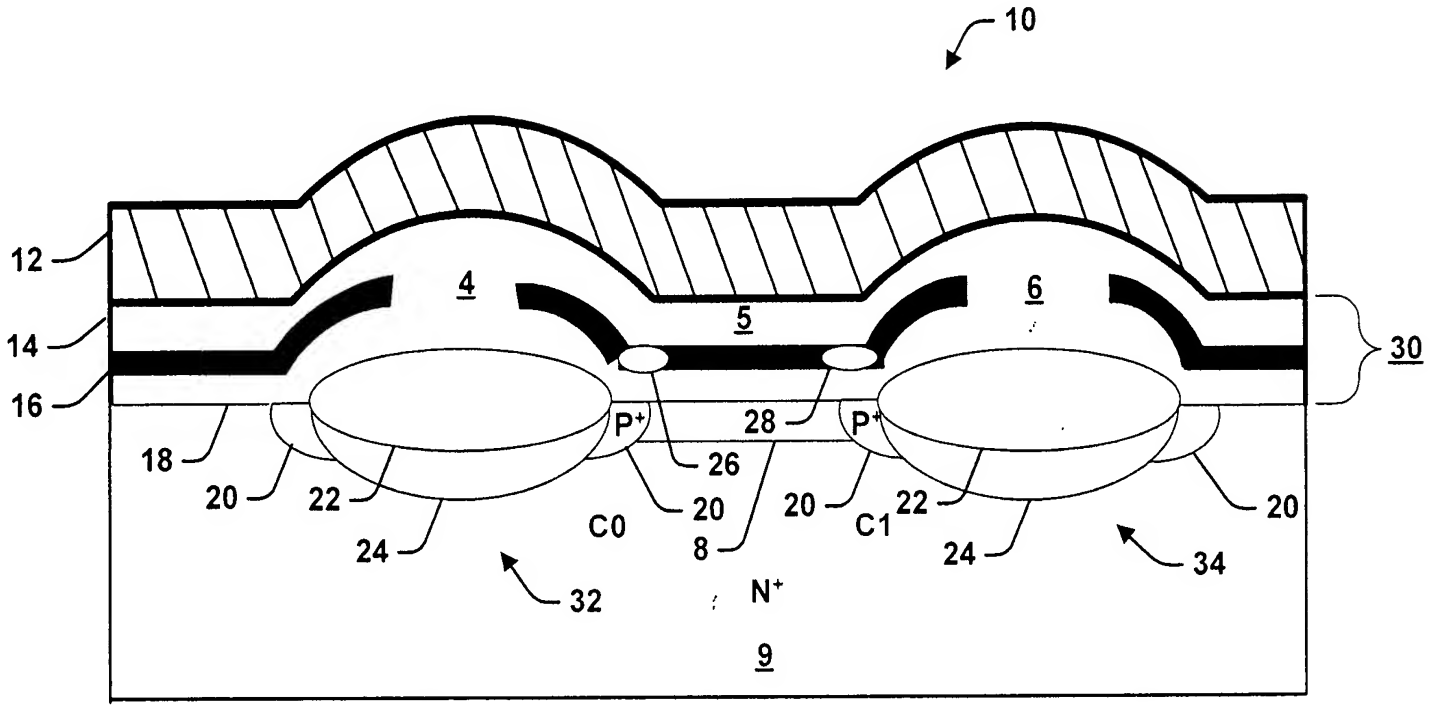

FIG. 1

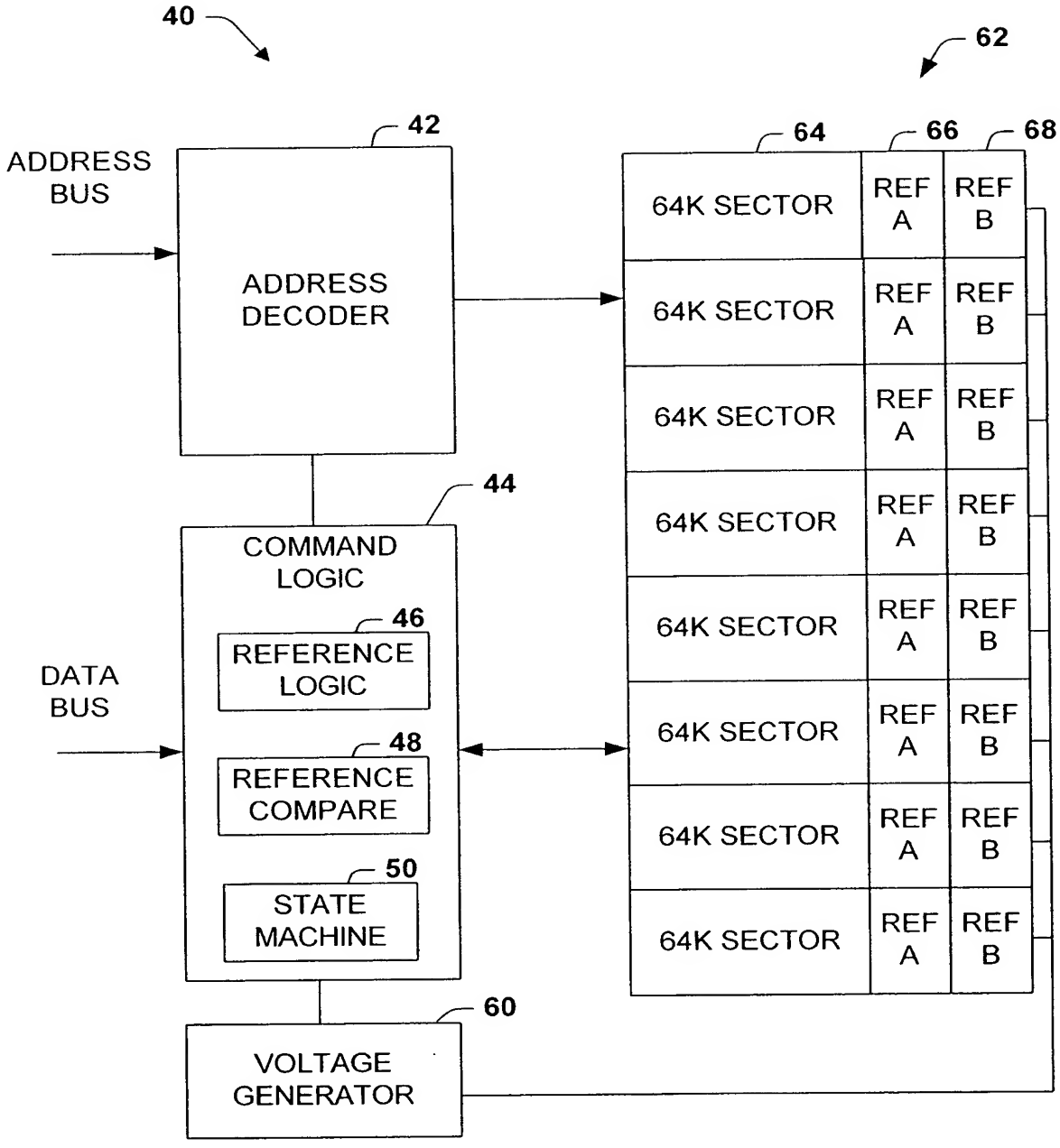
40
62
42
64
66
68
ADDRESS BUS
ADDRESS DECODER
64K SECTOR
REF A
REF B
44
COMMAND LOGIC
46
REFERENCE LOGIC
DATA BUS
48
REFERENCE COMPARE
50
STATE MACHINE
60
VOLTAGE GENERATOR

FIG. 2

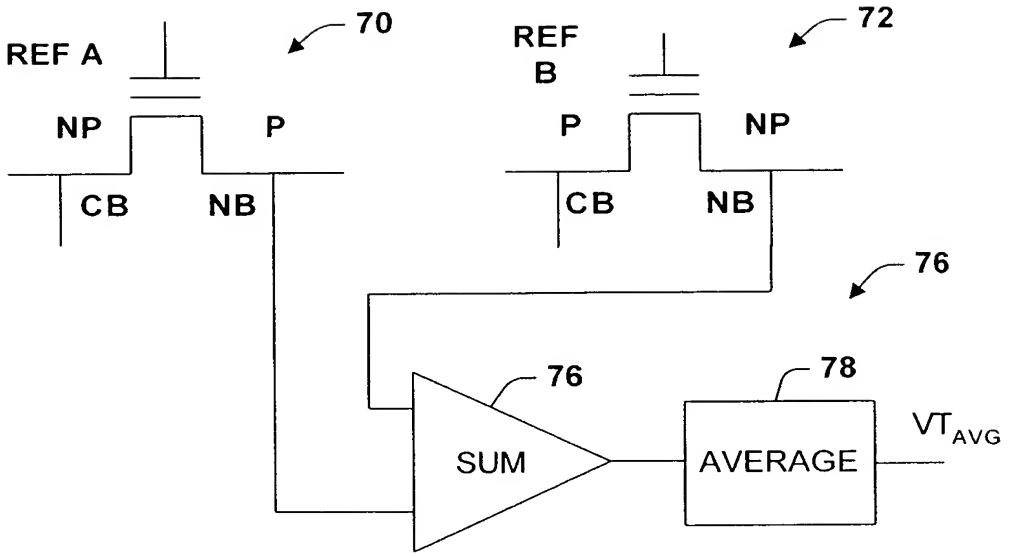
REF A
70
NP
P
CB
NB
REF
B
72
P
NP
CB
NB
76
76
78
SUM
AVERAGE
VT_{AVG}

FIG. 3

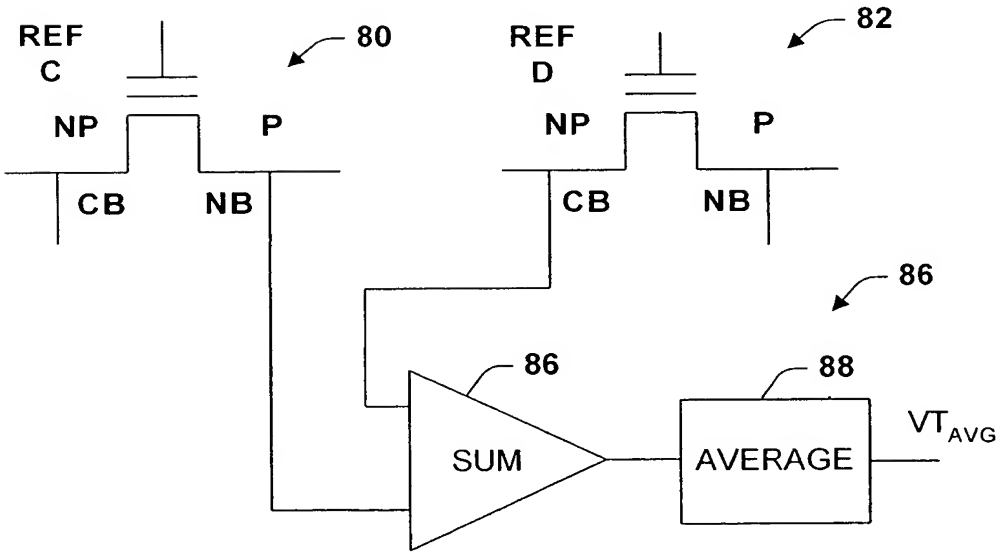
REF
C
80
NP
P
CB
NB
REF
D
82
NP
P
CB
NB
86
86
88
SUM
AVERAGE
VT_{AVG}

FIG. 4

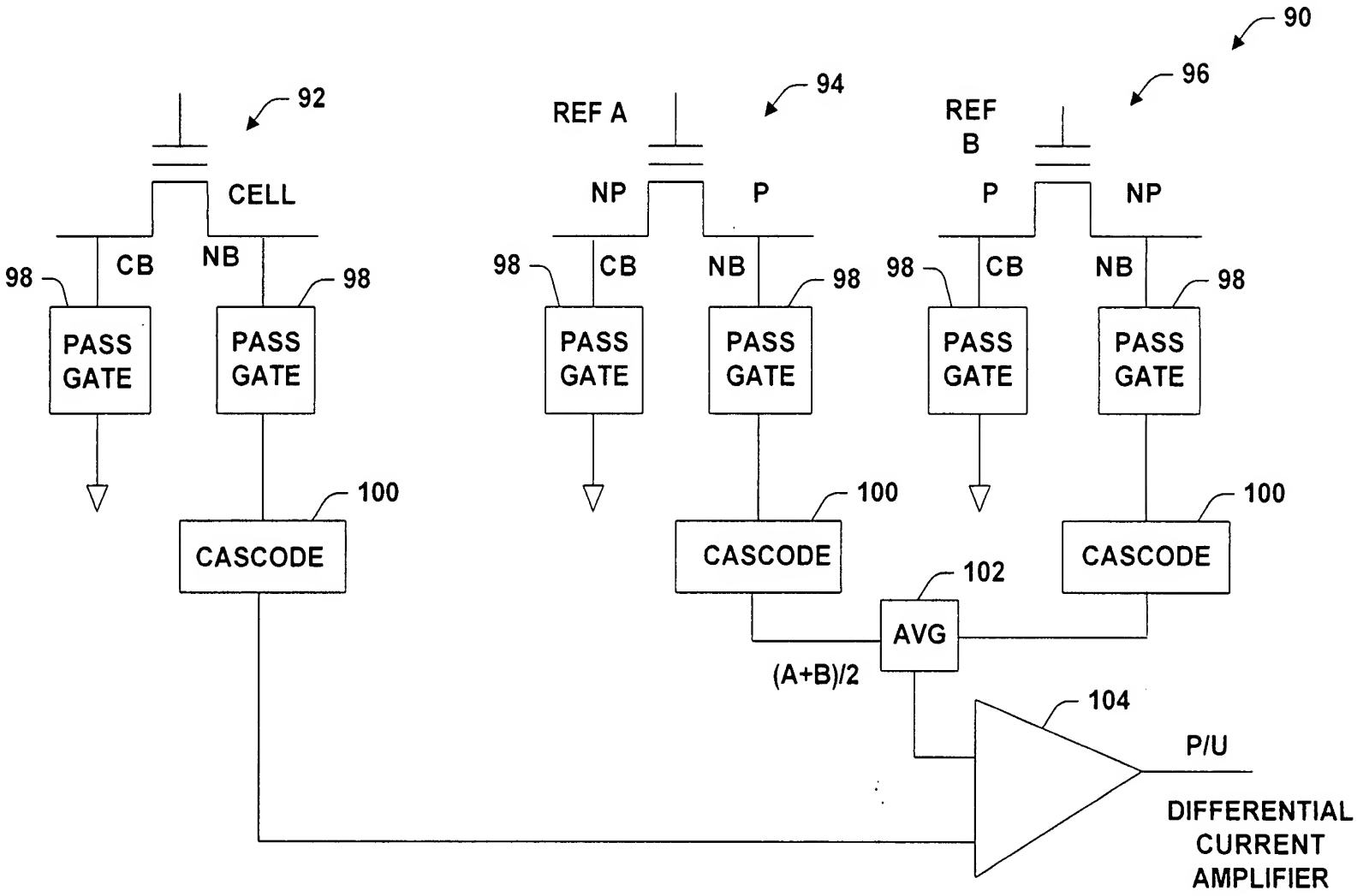
90
92
94
96
REF A
REF B
CELL
NP
P
P
NP
98
CB
NB
98
PASS GATE
PASS GATE
100
CASCODE
102
AVG
(A+B)/2
104
P/U
DIFFERENTIAL CURRENT AMPLIFIER

FIG. 5

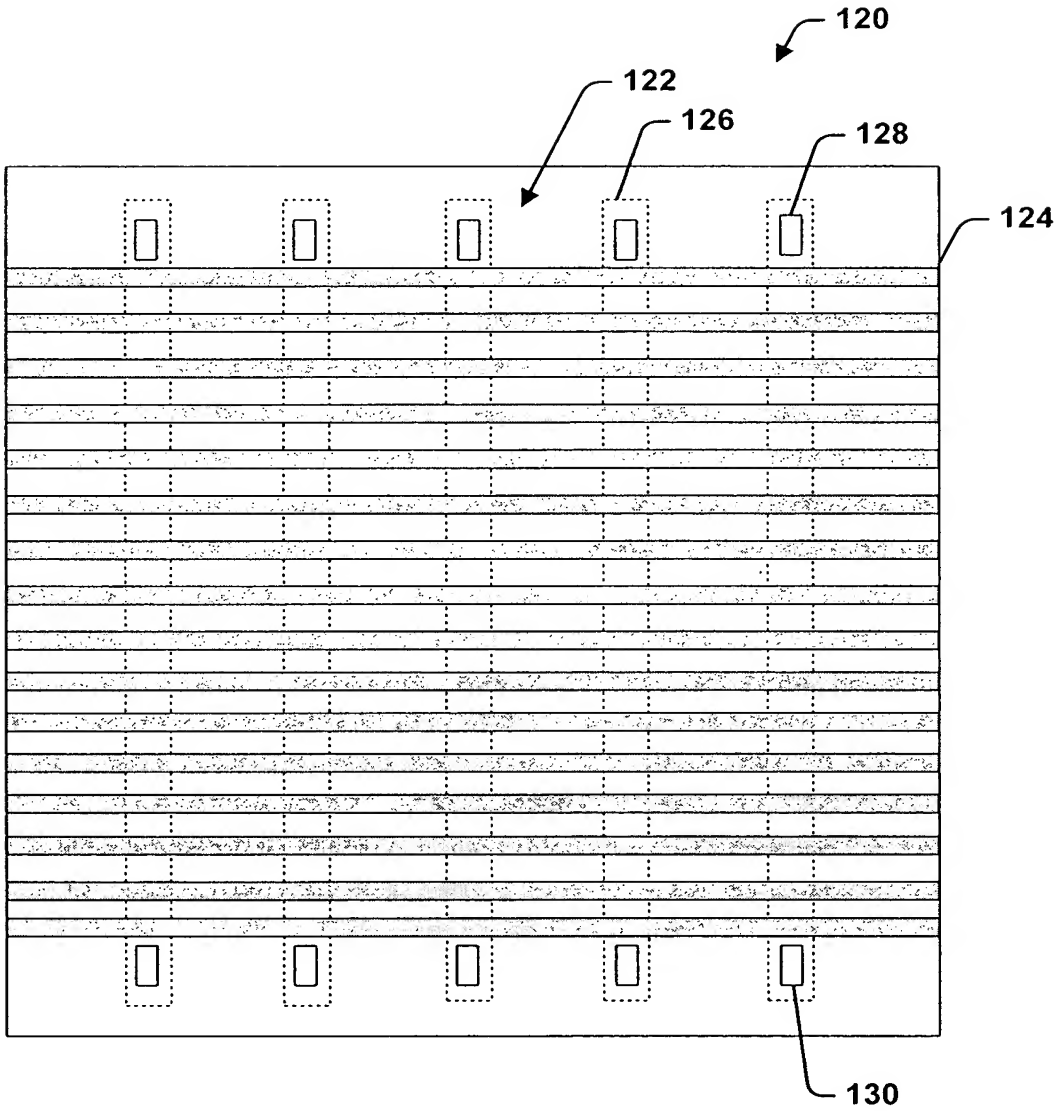

FIG. 6

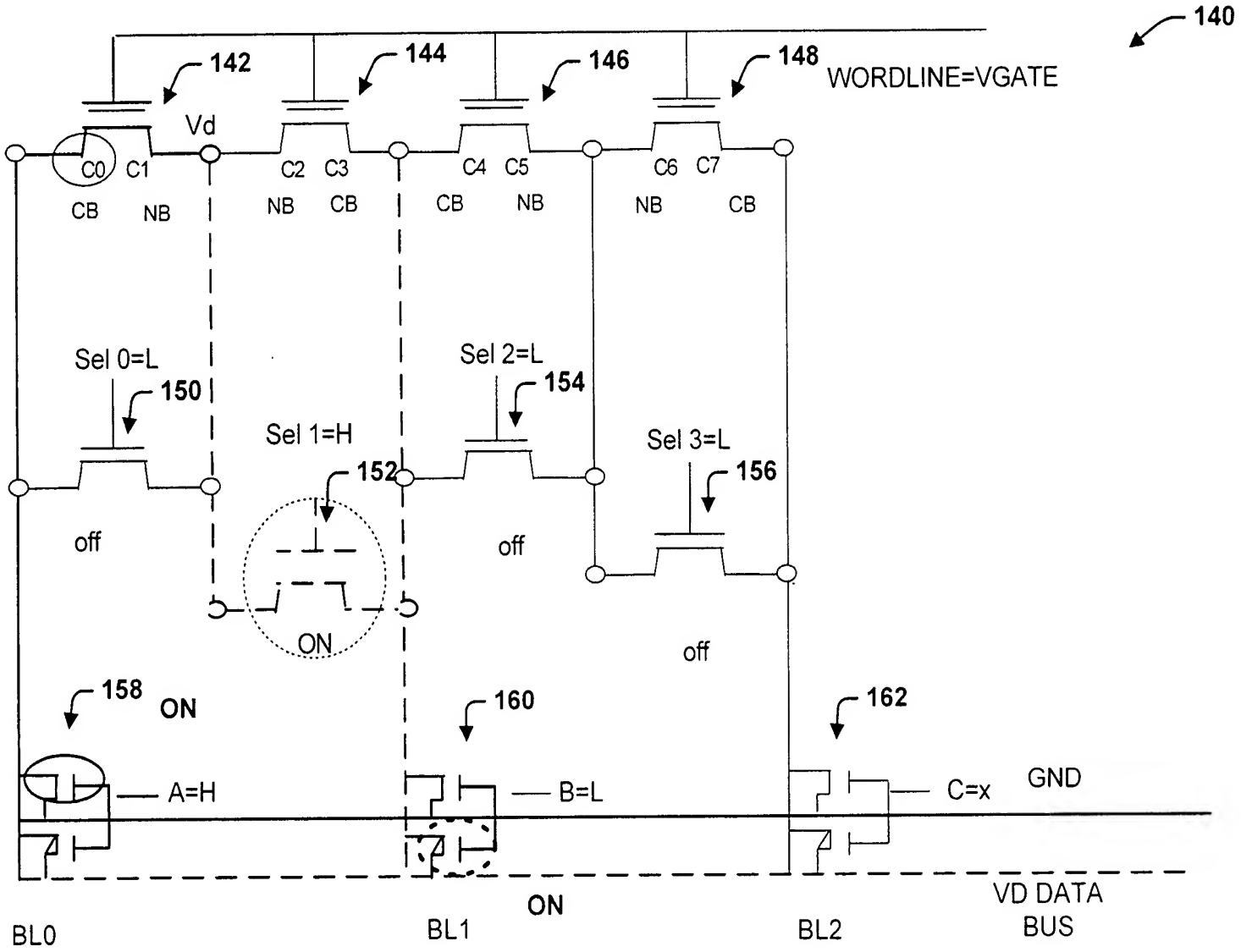
140
142
144
146
148
WORDLINE=VGATE
Vd
C0
C1
C2
C3
C4
C5
C6
C7
CB
NB
NB
CB
CB
NB
NB
CB
Sel 0=L
150
Sel 1=H
152
Sel 2=L
154
Sel 3=L
156
off
ON
off
off
158
ON
160
162
A=H
B=L
C=x
GND
ON
BL0
BL1
BL2
VD DATA
BUS

FIG. 7

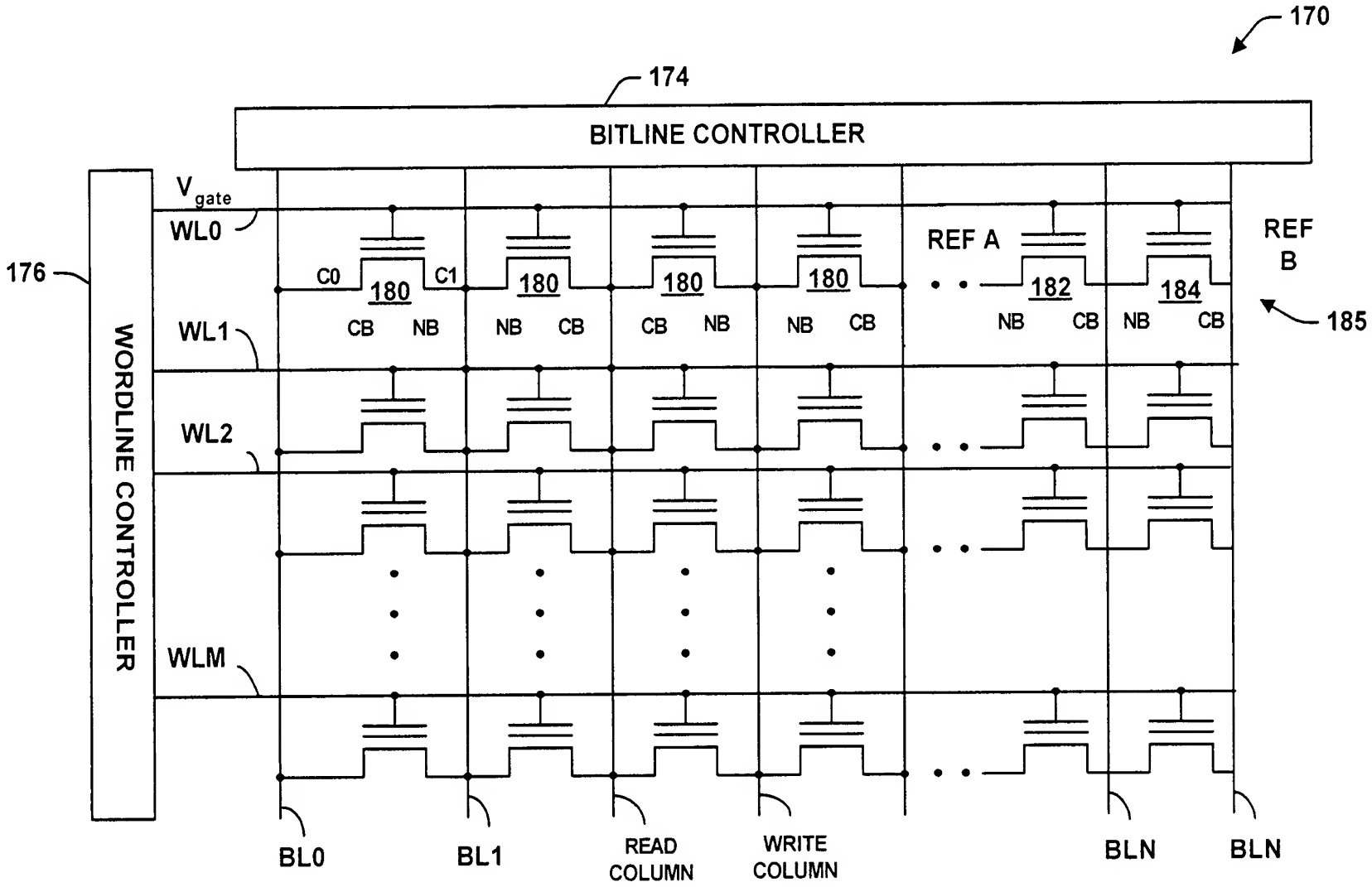
170
174
BITLINE CONTROLLER
176
WORDLINE CONTROLLER
V_{gate}
WL0
WL1
WL2
WLM
C0
C1
180
CB
NB
REF A
182
REF B
184
185
BL0
BL1
READ COLUMN
WRITE COLUMN
BLN
BLN
172

FIG. 8

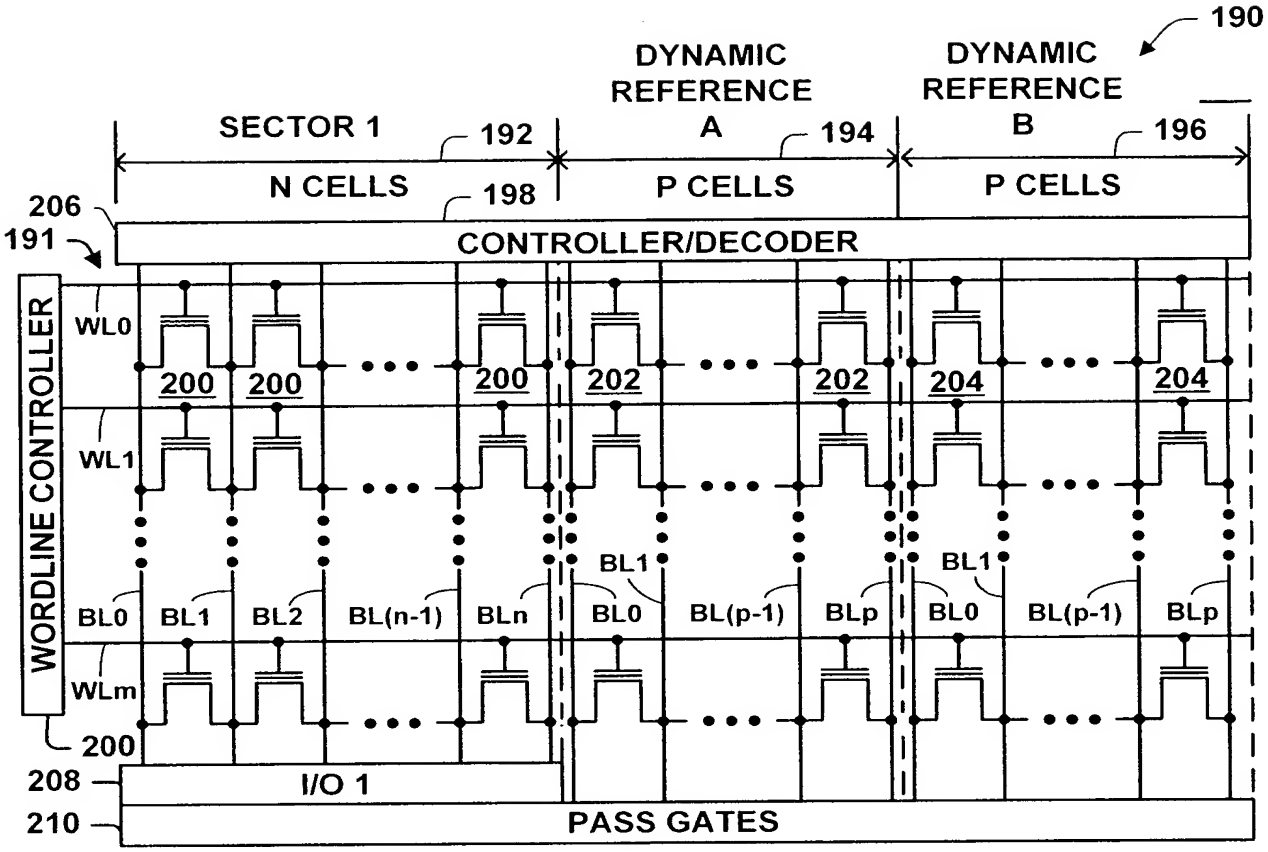
190
DYNAMIC REFERENCE A
DYNAMIC REFERENCE B
SECTOR 1
192
194
196
N CELLS
198
P CELLS
P CELLS
206
191
CONTROLLER/DECODER
WORDLINE CONTROLLER
WL0
WL1
WLm
200
200
200
202
202
204
204
BL0
BL1
BL2
BL(n-1)
BLn
BL0
BL(p-1)
BLp
BL0
BL(p-1)
BLp
BL1
BL1
200
208
I/O 1
210
PASS GATES

FIG. 9

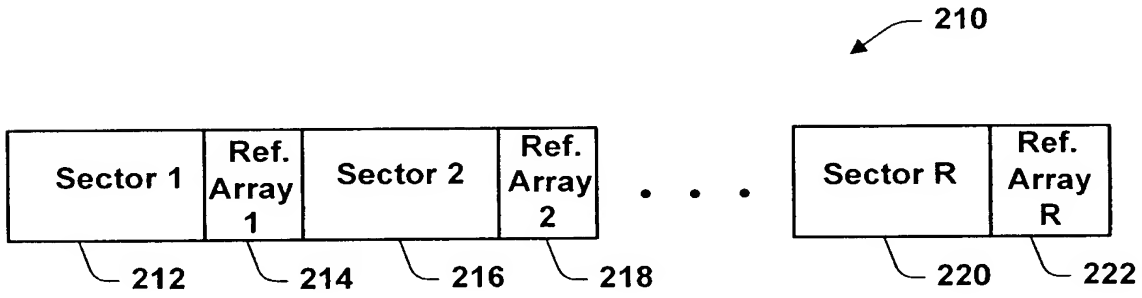
210
Sector 1
Ref. Array 1
Sector 2
Ref. Array 2
Sector R
Ref. Array R
212
214
216
218
220
222

FIG. 10

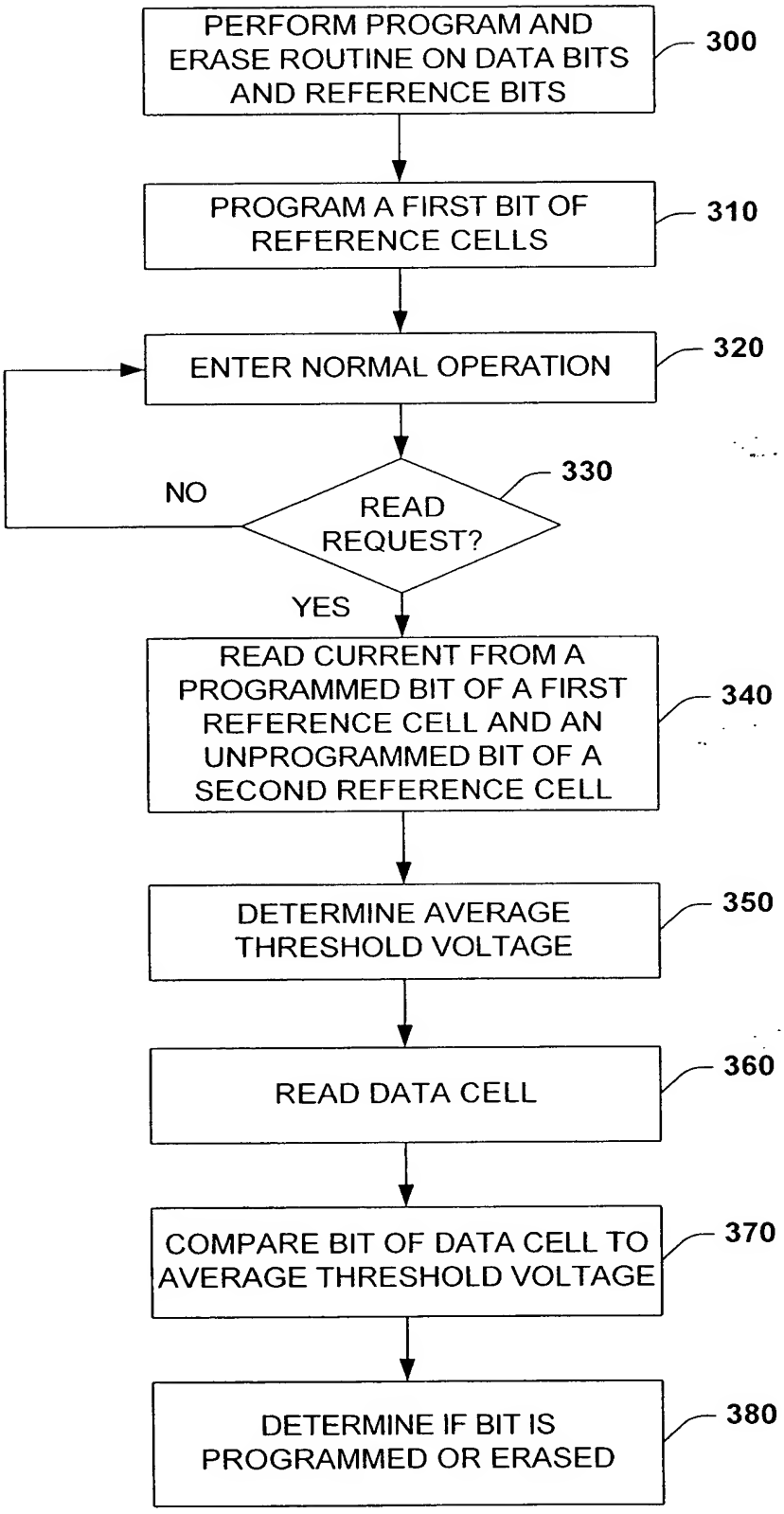
PERFORM PROGRAM AND ERASE ROUTINE ON DATA BITS AND REFERENCE BITS
300
PROGRAM A FIRST BIT OF REFERENCE CELLS
310
ENTER NORMAL OPERATION
320
NO
READ REQUEST?
330
YES
READ CURRENT FROM A PROGRAMMED BIT OF A FIRST REFERENCE CELL AND AN UNPROGRAMMED BIT OF A SECOND REFERENCE CELL
340
DETERMINE AVERAGE THRESHOLD VOLTAGE
350
READ DATA CELL
360
COMPARE BIT OF DATA CELL TO AVERAGE THRESHOLD VOLTAGE
370
DETERMINE IF BIT IS PROGRAMMED OR ERASED
380

FIG. 11

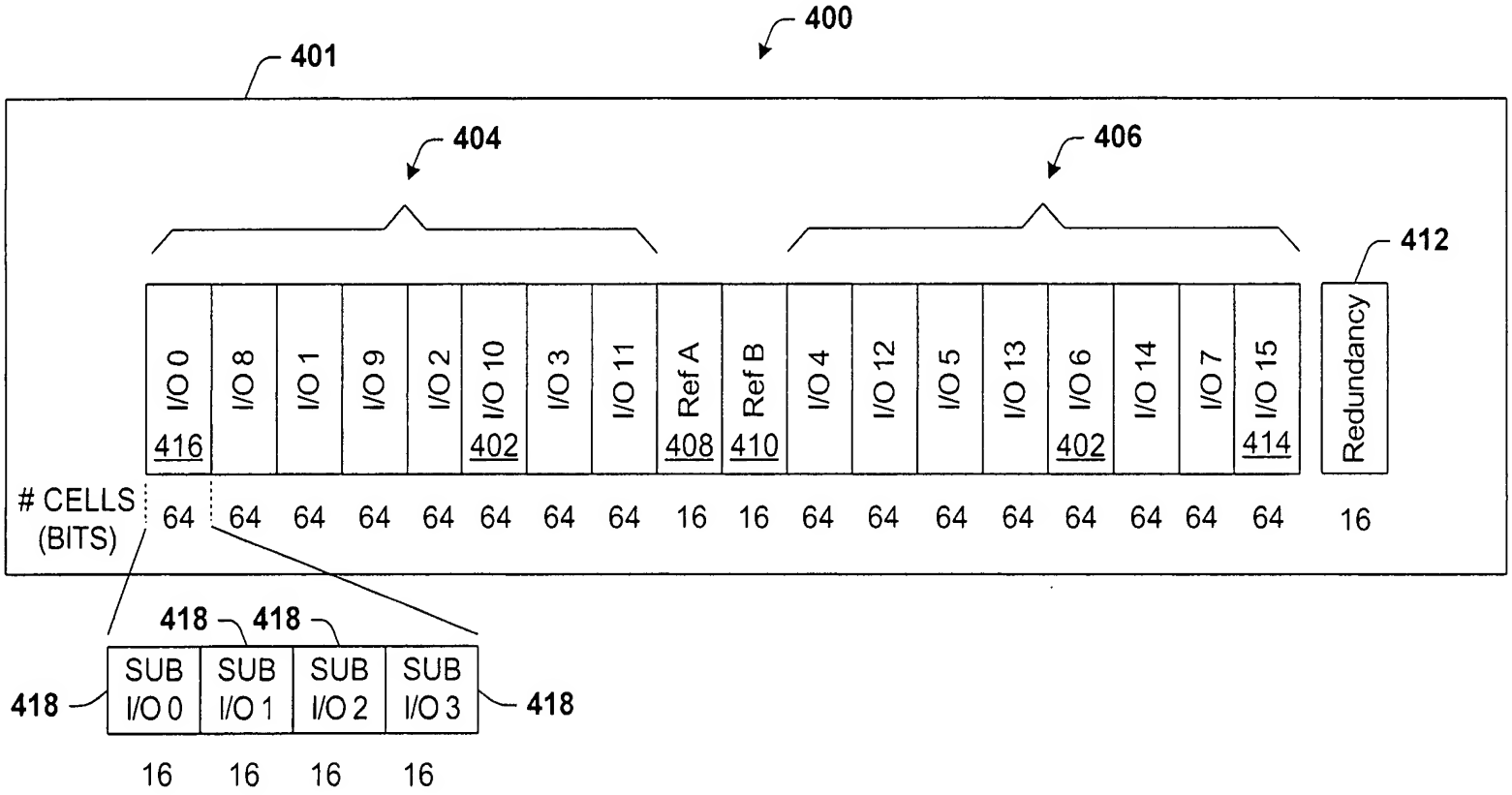
400
401
404
406
412
I/O 0
416
I/O 8
I/O 1
I/O 9
I/O 2
I/O 10
402
I/O 3
I/O 11
Ref A
408
Ref B
410
I/O 4
I/O 12
I/O 5
I/O 13
I/O 6
402
I/O 14
I/O 7
I/O 15
414
Redundancy
CELLS (BITS)
64 64 64 64 64 64 64 64 16 16 64 64 64 64 64 64 64 64 16
418 418
418
SUB I/O 0
SUB I/O 1
SUB I/O 2
SUB I/O 3
418
16 16 16 16

FIG. 12

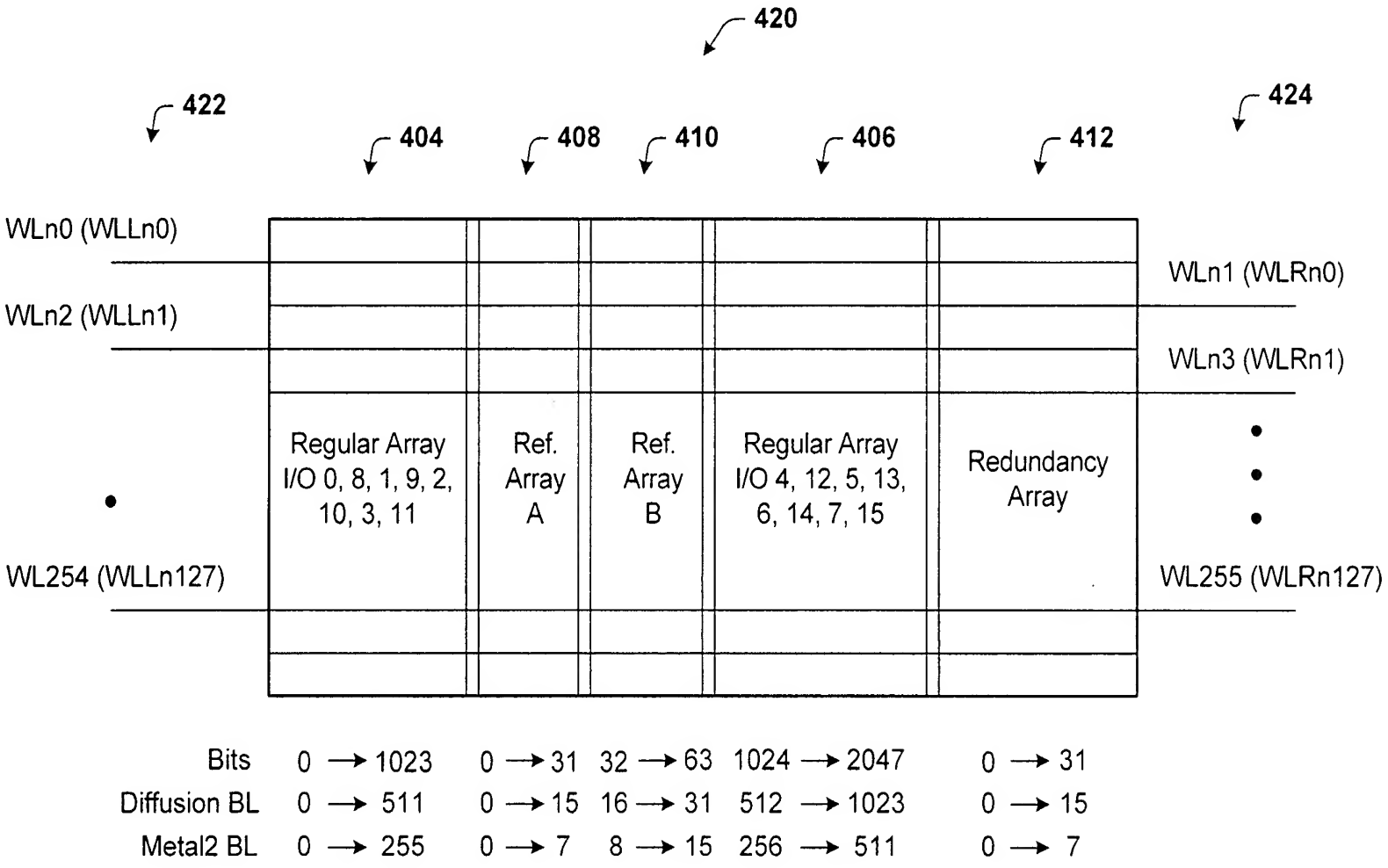
420
422
424
404
408
410
406
412
WLn0 (WLLn0)
WLn1 (WLRn0)
WLn2 (WLLn1)
WLn3 (WLRn1)
Regular Array I/O 0, 8, 1, 9, 2, 10, 3, 11
Ref. Array A
Ref. Array B
Regular Array I/O 4, 12, 5, 13, 6, 14, 7, 15
Redundancy Array
WL254 (WLLn127)
WL255 (WLRn127)
Bits 0 → 1023 0 → 31 32 → 63 1024 → 2047 0 → 31
Diffusion BL 0 → 511 0 → 15 16 → 31 512 → 1023 0 → 15
Metal2 BL 0 → 255 0 → 7 8 → 15 256 → 511 0 → 7

FIG. 13

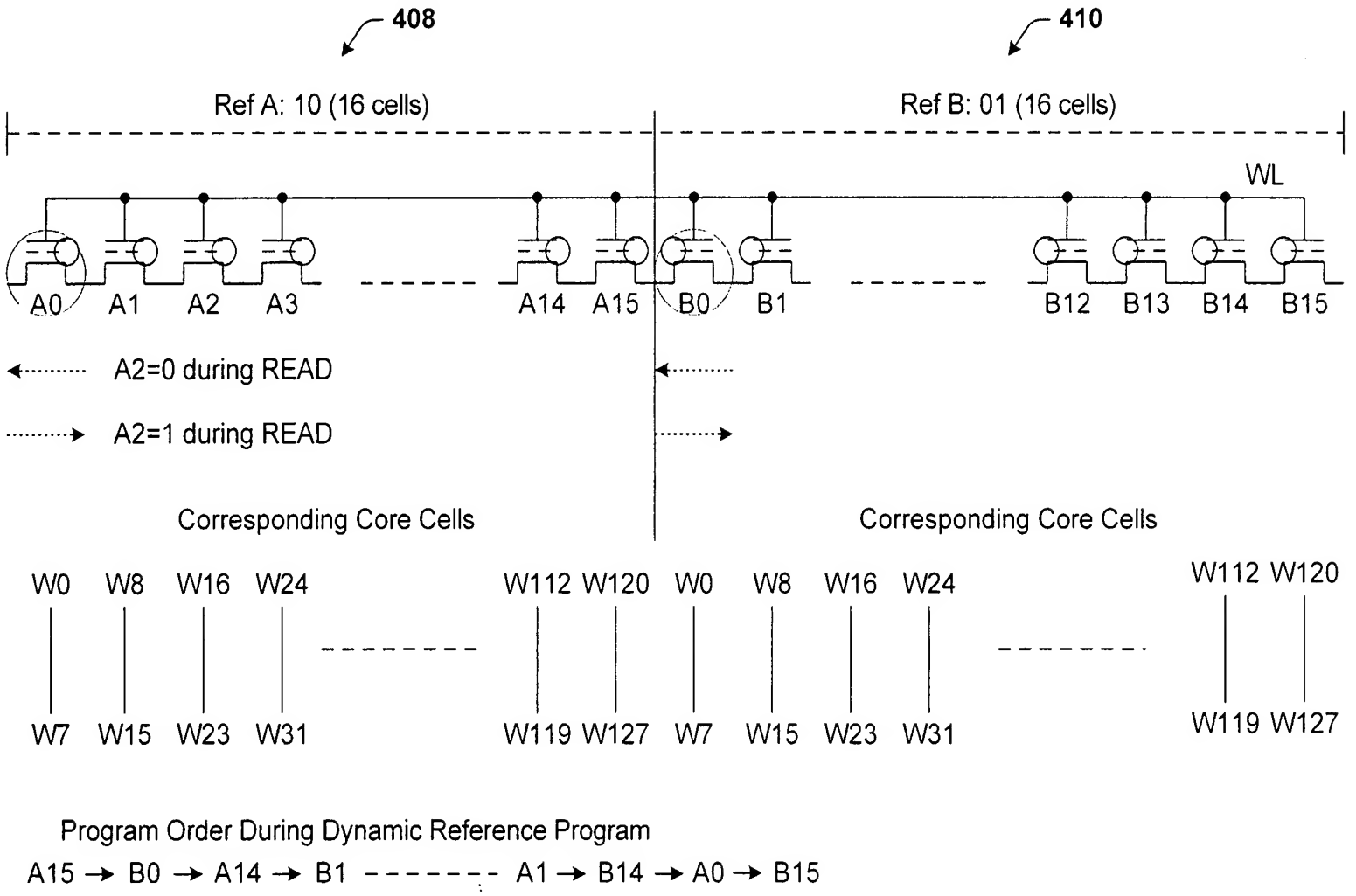
408
410
Ref A: 10 (16 cells)
Ref B: 01 (16 cells)
WL
A0
A1
A2
A3
A14
A15
B0
B1
B12
B13
B14
B15
A2=0 during READ
A2=1 during READ
Corresponding Core Cells
Corresponding Core Cells
W0
W8
W16
W24
W112
W120
W0
W8
W16
W24
W112
W120
W7
W15
W23
W31
W119
W127
W7
W15
W23
W31
W119
W127
Program Order During Dynamic Reference Program
A15 → B0 → A14 → B1 ------- A1 → B14 → A0 → B15

FIG. 14